2013 NDIA GROUND VEHICLE SYSTEMS ENGINEERING AND TECHNOLOGY SYMPOSIUM Systems Engineering (SE) Mini-Symposium August 21-22, 2013 - Troy, Michigan

Approved for Public Release, Distribution Unlimited

New DFR Method Captures All Critical Failure Modes into FMEA in Half the Time

(more time to focus on recommended actions and verification testing)

Howard C Cooper, DFSS-BB

Dmitry Tananko, PhD

DFR Reliability Engineer General Dynamics L.S. Sterling Heights, MI Manager Reliability General Dynamics L.S. Sterling Heights, MI

J. Gordon Shutek

Senior Director of Systems Engineering & Development General Dynamics Land Systems Sterling Heights, MI

ABSTRACT

Situation: There are many advantages during development of a design that come from doing Design Failure Mode Effects Analysis (DFMEA). These advantages include more reliable, safer, self-diagnosing, designs with higher Availability. Strictly from a Design for Reliability (DFR) viewpoint, DFMEA is the key tool to; a. identify and prioritize most critical potential Failure Modes (FMs) of the design, before design development, b. Document critical FM effects and root causes, and c. facilitate corrective actions and DVP&R planning, and d. form a reliability model which can be used to track reliability over the life of the design.

Problem: Since even small and simple designs often have a few hundred potential failure modes, preparing a good DFMEA is always a problem of Effectiveness vs., Efficiency. Traditionally it has been very hard to achieve Effectiveness when limited time, money and resources are available and the push for Efficiency, speed or deadlines, causes critical FMs to be missed all together. Likewise, Efficiency is hard to achieve due to the large number of potential FMs for each Subsystem. DFMEA preparation time can easily consumes 50 - 80 hours, or more, for both Reliability and for Design Engineers.

Solution Method & Tool: This paper presents for the first time, the "Function-to-Hardware Decomposition Table", a simple method for systematically capturing all potential failure modes into an FMEA. It establishes confidence that failure modes are not being missed or overlooked in the FMEA. One can also use of the Function-to-Hardware Decomposition Table (FH-Decomp) to prioritize all subsystem (hardware) functions, further improving confidence of a trustworthy FMEA methodology and places focus on critical failure mode root causes and mitigating actions, to improve reliability. Presented are two forms of the FH-Decomp Table and how to use them to achieve the above three benefits to DFR and to DFMEA preparation activities.

INTRODUCTION

Design Failure Mode Effects Analysis (DFMEA) is useful, even central to Design for Reliability (DFR) activities, yet DFMEA and FMEA are contested as often being too time consuming with sketchy or minimal results. Why do we do DFMEA? 'To be used as a living legal document? Or, to provide as a contract deliverable? Whatever your reason, a methodology is needed to more efficiently and effectively prepare the DFMEA without missing any potentially critical failure modes (FMs). Over the past three years, a structured methodology has been developed at General Dynamics, to accomplish this increased efficiency and effectiveness to develop a more trustworthy DFMEA. This methodology centers on first creating a simple Function-to-Hardware Decomposition Table or (FH-Decomp). Without such a tool, many DFMEA and FMECAs are simply a list of previously seen failures

(problems) on similar systems, with no understanding or inclusion of potential, unseen FMs. Other FMEAs are easily manipulated to look good, by artificially lowering likelihood and/or detection scores, to make the Risk Priority Number (RPN) look good. Such practices generate hard to detect, ineffective DFMEAs. Without the use of a structured FH-Decomp, DFMEA or FMEA have no gage or accountability for structure, flow, scoring rational, nor to insure all FMs are identified. The "FH-Decomp" provides accountability, thus the DFMEA becomes a trustworthy tool to effect reliability growth while mitigating critical "seen" and/or "unseen" potential failure modes.

Originally proposed as a way to show the relationship between a system's "ideal (output) functions" and the DFMEA "Items" or hardware subsystem's functional failure modes, the "FH-Decomp" has evolved into an efficient and effective way to prepare for DFMEA, to:

Insure all Hardware-Functions are identified

Insure all failure modes are identified,

Organize and structure the DFMEA,

Set relative likelihood of hardware item failures,

Understand system function failure severity depending on loss of the hardware functions,

Set relative criticality of each hardware-function, and

Prioritized selection of critical hardware-functions for inclusion and further investigation in the DFMEA (optional).

BACKGROUND

The key purposes for creating a DFMEA are to;

Create a reliability model of potential Failure Modes (FMs),

Identify and prioritize the most critical FMs of a design, during or before design development, and

Document critical FM effects and root causes, to facilitate corrective actions into the design and/or identify design verification tests (DVT), to detect critical failure modes and verify the design robust enough to function under the intended loads, through the intended environments with acceptable reliability.

The problem of generating a good DFMEA is always an Effectiveness vs. Efficiency Problem. A push for Efficiency, "speed" or to" meet deadlines" causes critical FMs to be missed, which means a loss of Effectiveness. Yet, a push for Effectiveness often results in an extremely large number of potential FMs for each Subsystem, consuming over 100 hours for both Reliability and for Design Engineers, to document all the potential failure modes they can think of, or identify, which causes a loss of Efficiency. Even then some potential failure modes (FMs) may be missed.

Solution to both the efficiency vs. effectiveness problem and to the problem of "missing FMs" are solved by first creating a Hardware to Function Decomposition Table (FH-Decomp), as shown in Figure 1, below.

Function to Hardwa	are Deco	mpositio	on Table			
"Design" Functions: (Ideal Functions from P- Diagram / Functions (lines crossing boundary of B-Diagram "Design".)	1. Transfer Exaust from Engine out of the Vehicle			2. Attenuate NVH	3. Limited thermal transfer to vehicle	5. Exhaust Brake Engine Slowing
Hardware Functions:	Secure	Contain Exhaust	Provide Flow	Attenuate NVH	Contain Heat	Partially Restrict Exhaust
Hardware:						
V-Band Clamps	Х					
Exaust Pipe		Х	Х			
Flat Flange	Х					
Seals		Х				
Muffler		Х	Х	X		
Insulation				X	X	
Isolation Mounts	X			X		
Exaust Brake		X	X			X
Flex Pipe		X	X			
Elbow		X	Х			

Figure 1: FH-Decomp identifies all hardware functions and potential failure modes

DEVELOP YOUR OWN "FH-Decomp"

An Function to Hardware Decomposition Table (FH-Decomp) can be formed from schematics drawings, design specification documents or any other sources that yield the design's intended (output) or "ideal functions" (see top row of FH-Decomp). Also, a document, or understanding is needed to list in the lefthand column the subsystems of this system or the hardware or sub-circuits that are one indenture level below the boundary of the system or design being analyzed. That's it.

The DFMEA team of SMEs will identify the "Hardware-Functions" (vertical) in the second row, above, as they discuss each hardware item's involvement or non-involvement ("X" or no "X") toward achieving the "Design" Function, in the upper

row. Insert the hardware-functions as the team works their way from left-to-right, identifying, with an "X", which hardware items are needed to perform the "Design" Function.

To most efficiently facilitate these steps, use a functional boundary block diagram (B-Diagram) shown below.



Figure 2: B-Diagram of Vehicle Exhaust System

Each line crossing into or out of the dotted line Boundary, reflects a system's or "Design's" Function. The B-Diagram also shows graphically, by name and in functional relationship, the Hardware items (one indenture level down) to be investigated in the DFMEA. These are first listed in the left-hand column of the FH-Decomp, as the Hardware items.

Not all system or "Design" Functions need go into the FH-Decomp, and thus into the DFMEA. The "Ideal Functions" or output functions from a P-Diagram are the needed functions to investigation in a DFMEA.



Figure 3: P-Diagram separates Input, Control and Ideal Functions

As seen in this P-Diagram model of a vehicle exhaust system, there are more "Ideal Functions" than output functions in Figure 2. The P-Diagram also helps to separate "Input" and "Control" Functions. These type functions are assumed perfect and fulfilled as they enter the Boundary Diagram boundary of investigation, so they do not go into the FH-Decomp. This shortens the DFMEA, keeping it focused on failure modes within the boundary. Yet, input interfaces, input devices and control hardware items within the boundary will be examined and when failed will effect one or more of the "Ideal Functions".

The P-Diagram is also helpful to the DFMEA as it captures the uncontrollable "Noise Factors" (see top section) or environmental root cause energies which can immediately or over time cause the bounded system (design) a loss of functionality and go into "Error State". One or more of these Noise Factors will be placed in the Cause column of the DFMEA for each failure mode (FM). And, the Error States will show up in DFMEA Next Level Effects column, for these FMs that would cause the Error State.

Yet, neither the B-Diagram, nor the P-Diagram has identified the hardware-functions, nor the failure modes of the subsystems or blocks within the B-Diagram. When we say, "Failure Mode Effects Analysis", these are the failure modes we are talking about. We need to capture these hardware-function failure modes, in a straight forward, structured way, into the DFMEA, so we do not miss critical failure modes (FMs). Error States or System "Design" Function FMs are the effect of the lower level hardware-function FMs.

Thus, we introduce the FH-Decomp as an effective tool to capture all hardware-functions. Each hardwarefunction will then translate to two, three, or four functional FMs, in the DFMEA:

Too much of the function

Too little of the function

Intermittent functioning

Total loss of the function

Inadvertent erroneous unintended functioning (as commanded by a Processor, computer, or from software).

Populating an FH-Decomp Table, one quickly realizes that hardware items serve more functions than one and are frequently needed to support more than one "Design" Function. Therefore more rows needed in the DFMEA, to be complete and trustworthy. However, we could reduce rows in the DFMEA, if the FH-Decomp could also prioritize hardware-functions, critical enough to be evaluated in the DFMEA?

PRIORITIZING CRITICALITY with FH-Decomp Table

By simply documenting relative likelihood of failure for each hardware item, below, and documenting worst case severity of loosing each hardware function, below, based on how it would impact the "Design" Function, each hardware-function's worst case criticality can be indicated rather than a simple "X". See hardwarefunction intersection cells below:



Figure 4: Criticality replaces X, in FH-Decomp Table

The definition of "Criticality" is, "the severity of an incident or action times the likelihood or rate of occurrence". Assuming we are simply wanting to analyze the most critical FMs of the "Design", then analyzing just "double digit critical" hardwarefunctions into the DFMEA provide a means to ignoring low, single digit critical hardware functions. Time saved documenting all the DFMEA detail on low criticality Failure Modes (FMs) allows time and attention on mitigating more critical FMs. The DFMEA further analyzes which of these critical hardware-functions will have critical or high RPN failure modes. One then observes that the actual FMs have the same or lower severity than posted in the FH-Decomp hardware-function. Also, actual FMs will have the same or lower OCC (Occurrence Likelihood) scores than posted against the hardware item, in the FH-Decomp. Yet, no DFMEA FM could have higher criticality than indicated in the FH-Decomp's hardware-function "cross cell". Therefore, according to the 80/20 rule or Pareto principle, capturing all the FM's into the DFMEA to analyze the 20% most critical hardware-functions of the FH-Decomp, you will be analyzing and mitigating the few FMs able to yield 80% of the reliability growth. 80% of the failures that would actually otherwise occur. Also, as is normally the case, when you mitigate the more critical FMs, you are actually mitigating the less critical FMs as well, because the means of mitigation (isolation, cushioning, lubricating, cooling, etc.) will also mitigate and positively affect neighboring hardware or similar FMs in the "design".

Sequence of Pre-DFMEA Design Description

The most direct path, then, to prepare and describe the design, its functions and its "hardware-functions", account for all FMs and prioritize DFMEA effort on the most critical FMS, is to:

Prepare a Boundary Diagram, then a P-Diagram and from these two, prepare a FH-Decomp Table.

Identify all hardware-functions

Identify Hardware likelihood of failure and hardware-function loss severity.

Let the FH-Decomp calculate Criticality

Populate the DFMEA with all, or with the most critical hardware-function FMs (see below)



From the FH-Decomp the DFMEA is structured and populated. Thus, the FH-Decomp serves as an index or audit trail for completeness, OCC likelihood scoring and to provide maximum hardware-function criticalities:



Figure 5: DFMEA filled out from FH-Decomp Table

Further, the information in FH-Decomp helps to set ceiling scores or values in the DFMEA Severity and Occurrence columns and "Noise Factors" from the P-Diagram serve as a resource when identifying each FM's root-cause in the Mechanism of Failure column.

Summary

The criticality prioritizing Function-to-Hardware Decomposition Table (FH-Decomp) was developed and used to facilitate Design for Reliability and DFMEA analysis on an entirely new Vehicle design, this past year, allowing the design team to move from

SFR to PDR in only 3 months. It provided time to identify recommended actions to mitigate the most critical failure modes on each critical subsystem, to close the reliability assessment vs., allocation and assure meeting the vehicle reliability requirements. The same amount of DFMEA work took at least 5 times the man-hours on previous programs. This prioritizing FH-Decomp method is now being used on other programs approaching PDR or CDR, Design Reviews. Design teams see the clear functional path into DFMEA and thus take ownership of their DFMEA and become interested in looking at ways to mitigate critical failure modes. The FH-Decomp table is also being used as a tool for Diagnostics to plan and prepare, earlier in the development cycle, a path to achieving Testability Requirements, as they quantify each Hardware items failure rate assessment and determine which hardwarefunctions they are able to detect and report upon failure of the system.

REFERENCES

[1] SAE 1739 FMEA Standards & Practice

[2] MIL-STD-1629a, FMECA Standards & Practice

BIOGRAPHY

Howard C Cooper is a Reliability Engineer for General Dynamics, facilitating engineering teams through the Design for Reliability (DFR) process. He is a Design for Six Sigma Black Belt, specialized at facilitating FMEA and TRIZ Structured Innovation. Previous to GDLS he worked DFR at GE Medical Systems and spent 26-years consulting on reliability issues for manufacturing automation controls and computer controlled machine tools. His focus was helping Fortune 500tm companies eliminate 70% - 92% of their unscheduled equipment downtime, in 30-60 days! He coined the phrase, FISH[™] (Functional Interface Stress Hardening), to explain how dramatic reliability improvement can be achieved during development and for fielded equipment. His seminar: "How To FISH − Eliminating 70-92% of Your Unscheduled Equipment Downtime in 30-60 Days" is often rated as "most valued seminar of my career" by operations, maintenance and plant engineers, manufacturing and plant managers. Mr. Cooper received a B.S. degree from SUU, in Math and Industrial Technology and did M.S. work in Technical Education at BYU.

Howard C Cooper, BS, DFSS-BB, TRIZ, DFR howard.c.cooper@gmail.com